

Yuzhe Fu

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EDUCATION

Peking University – Beijing, China

September 2021 – June 2024

Master in Microelectronics and Solid-State Electronics

- GPA: 3.59 / 4.0
- Supervisor: Prof. Hailong Jiao

University of California, Berkeley – Berkeley, USA

August 2019 – Dec 2019

Semester Exchange, Global Access Program

- GPA: 3.94 / 4.0

Southern University of Science and Technology – Shenzhen, China

September 2017 – June 2021

Bachelor of Microelectronics Science and Engineering

- GPA: 3.88 / 4.0, **1st in Comprehensive Ranking**
- Supervisor: Prof. Fengwei An

RESEARCH INTERESTS

- Algorithm-hardware co-design
- Energy-efficient and configurable artificial intelligence accelerator design

PUBLICATIONS

- **Y. Fu**, C. Zhou, T. Huang, E. Han, Y. He, and H. Jiao, "[SoftAct: A High-Precision Softmax Architecture for Transformers with Nonlinear Functions Support](#)," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, 2023. (Under peer-review)
- C. Zhou#, **Y. Fu**#, Y. Ma, E. Han, Y. He, and H. Jiao, "[Adjustable Multi-Stream Block-Wise Farthest Point Sampling Acceleration in Point Cloud Analysis](#)," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, 2023. (# Authors with equal contribution, under second revision)
- C. Zhou, **Y. Fu**, M. Liu, S. Qiu, G. Li, Y. He, and H. Jiao, "[An Energy-Efficient 3D Point Cloud Neural Network Accelerator with Efficient Filter Pruning, MLP Fusion, and Dual-Stream Sampling](#)," *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2023. [\[YouTube\]](#)
- C. Zhou, M. Liu, S. Qiu, X. Cao, **Y. Fu**, Y. He, and H. Jiao, "[Sagitta: An Energy-Efficient Sparse 3D-CNN Accelerator for Real-Time 3D Understanding](#)," *IEEE Internet of Things Journal (IoTJ)*, 2023.
- P. Dong, Z. Chen, Z. Li, **Y. Fu**, L. Chen, F. An, "[A 4.29nJ/pixel Stereo-depth Coprocessor with Pixel-level Pipeline and Region-Optimized Semi-Global Matching for IoT Application](#)," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, 2021.

PATENTS

- F. An, **Y. Fu**, P. Dong, Z. Chen, Z. Li, "[Low-power-consumption stereo matching system and method for acquiring depth information](#)," *CN Patent*, 2020, CN112070821A / WO2022021912A1.

TAPE OUT

- An energy-efficient pipelined and configurable 3D point cloud-based neural network accelerator was fabricated in TSMC 28-nm HPC technology with an area of 2.0 mm×1.5 mm in July 2023.
- A 4.5 TOPS/W sparse 3D-CNN accelerator for real-time 3D understanding was fabricated in UMC 55-nm low-power CMOS technology with an area of 4.2 mm×3.6 mm in August 2020.

SKILLS

- Proficient in digital integrated circuit development (RTL implementation and logic synthesis), FPGA development, and neural network model training and compression.
- Familiar tools: Vivado/Quartus, Cadence (Genus and NCSim); PyTorch, Intel Distiller (model compression).
- Knowledgeable languages: Verilog HDL, Python, JAVA, MATLAB, Shell, Makefile.
- I am an easygoing and self-motivated person with a positive attitude to life.

RESEARCH EXPERIENCE

SoftAct: A High-Precision Softmax Architecture for Transformers Supporting Nonlinear Functions

Project Leader

July 2022 – Present

- Developed an improved softmax with penalties and optimized precision.
- Introduced a full-zero-detection method and designed a compact and reconfigurable architecture.
- Implemented in TSMC 28nm technology and benchmarked with the MobileViT network, improving up to 5.87% network accuracy, 153.2× area efficiency, and 1435× overall efficiency.

Farthest Point Sampling Acceleration for Point Neural Network

Project Leader

February 2022 – Present

- Proposed an adjustable multi-stream block-wise FPS, ensuring precision and reducing 99.9% latency.
- Developed a pre-evaluation method to select optimal configurations without network training.
- Implemented in TSMC 28nm technology, achieving up to 99.5% energy saving and 9.34% network accuracy improvement.
- Now implementing in CUDA to speed up PNN training on GPUs.

Nebula: An Energy-Efficient 3D Point Cloud-Based Neural Network Accelerator

Main Contributor & Module Leader

February 2022 – Present

- Responsible for network work (model training, quantization, pruning, algorithm verification, etc.).
- Proposed a novel FPS accelerating unit, ensuring precision while mitigating complexity by 14.22×.
- Co-designed a block-wise MLP fusion dataflow scheme, reducing the memory access by 21.1×.
- Now building an FPGA-based chip testing platform for further submission.

Sagitta: An Energy-Efficient Sparse 3D-CNN Accelerator for Real-Time 3D Understanding

Contributor

December 2021 – December 2022

- Responsible for pruning and extraction of network data for analysis.
- Leveraged locality and small differential value dropout to increase the sparsity of activations.

SGM Accelerator: A 4.29nJ/pixel Stereo-depth Coprocessor with Pixel-level Pipeline and Region-Optimized Semi-Global Matching for IoT Application

Project Leader

February 2020 – June 2021

- Proposed a region-optimized stereo matching strategy improving the speed of traditional semi-global matching algorithm by 5× while ensuring accuracy.
- Proposed a four-layer parallel pipeline hardware architecture and implemented it on FPGA platform which can extract depth information in real-time at 156 MHz and 508 fps under VGA resolution.

HONORS & AWARDS

- Excellent Graduate Award, Southern University of Science and Technology, 2021
- Outstanding Graduate Award, School of Microelectronics in SUSTech, 2021
- Best Presentation Award, IEEE CASS Shanghai and Shenzhen Joint Workshop, 2021
- **National Scholarship (the highest scholarship for Chinese undergraduates)**, 2020
- Shenzhen Longsys Electronics Company Award (**Top 2% in School of Microelectronics**), 2020
- Excellent Student Volunteer, SUSTech Global Engagement Office, 2020
- First Class Scholarship (**top 5% in SUSTech**), *Southern University of Science and Technology*, 2019
- First Class Scholarship (**top 5% in SUSTech**), *Southern University of Science and Technology*, 2018